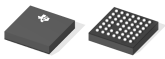


SBAS265 – OCTOBER 2002

Low Voltage I/O TOUCH SCREEN CONTROLLER

FEATURES

- SAME PINOUT AS ADS7846
- 2.2V TO 5.25V OPERATION
- 1.5V TO 5.25V DIGITAL I/O
- INTERNAL 2.5V REFERENCE
- DIRECT BATTERY MEASUREMENT (0V to 6V)
- ON-CHIP TEMPERATURE MEASUREMENT
- TOUCH-PRESSURE MEASUREMENT
- QSPI™, SPI™ 3-WIRE INTERFACE
- AUTO POWER-DOWN
- AVAILABLE IN THE VFBGA-48 PACKAGE

APPLICATIONS

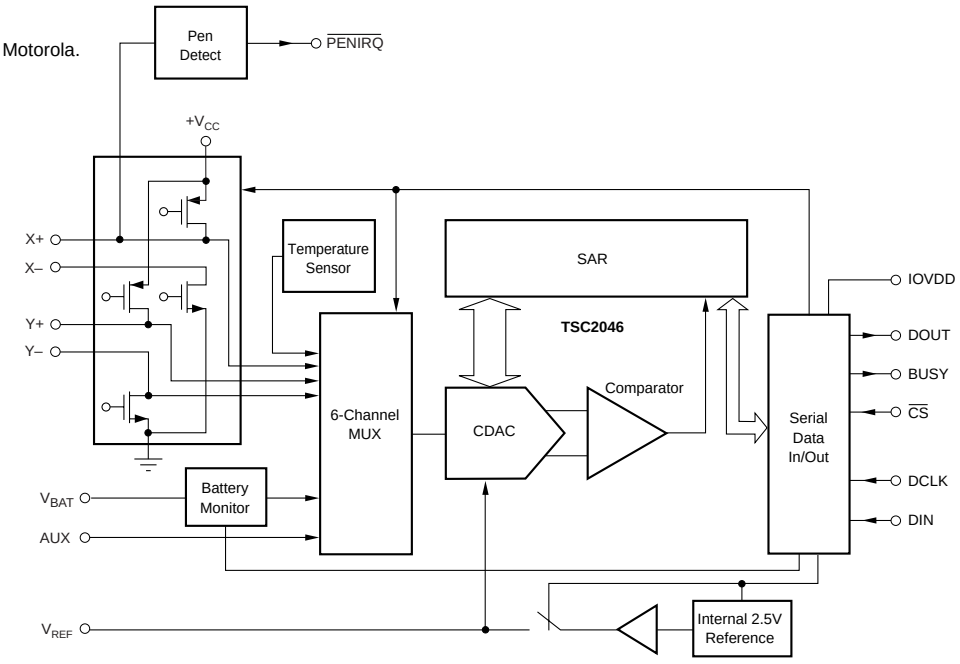
- PERSONAL DIGITAL ASSISTANTS
- PORTABLE INSTRUMENTS
- POINT-OF-SALE TERMINALS
- PAGERS
- TOUCH SCREEN MONITORS
- CELLULAR PHONES

QSPI and SPI are registered trademarks of Motorola.

DESCRIPTION

The TSC2046 is a next-generation version to the ADS7846 4-wire touch screen controller which supports a low-voltage I/O interface from 1.5V to 5.25V. The TSC2046 is 100% pin-compatible with the existing ADS7846, and will drop into the same socket. This allows for easy upgrade of current applications to the new version. The TSC2046 also has an on-chip 2.5V reference that can be utilized for the auxiliary input, battery monitor, and temperature measurement modes. The reference can also be powered down when not used to conserve power. The internal reference will operate down to 2.7V supply voltage, while monitoring the battery voltage from 0V to 6V.

The low power consumption of < 0.75mW typ at 2.7V (reference OFF), high-speed (up to 125kHz sample rate), and on-chip drivers make the TSC2046 an ideal choice for battery-operated systems such as Personal Digital Assistants (PDAs) with resistive touch screens, pagers, cellular phones, and other portable equipment. The TSC2046 is available in the VFBGA-48 package and is specified over the –40°C to +85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ and IOVDD to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to IOVDD + 0.3V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2046	±2	VFBGA-48	GQC	–40°C to +85°C	AZ2046	TSC2046IGQCR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = 2.5V internal voltage, f_{SAMPLE} = 125kHz, f_{CLK} = 16 • f_{SAMPLE} = 2MHz, 12-bit mode, digital inputs = GND or IOVDD, and $+V_{CC}$ must be ≥ IOVDD, unless otherwise noted.

		TSC2046			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Full-Scale Input Span	Positive Input-Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ + 0.2	V
	Negative Input	–0.2		+0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB[1]
Offset Error				±6	LSB
Gain Error	External V_{REF}			±4	LSB
Noise	Including Internal V_{REF}		70		µVrms
Power-Supply Rejection			70		dB
SAMPLING DYNAMICS					
Conversion Time				12	CLK Cycles
Acquisition Time		3			CLK Cycles
Throughput Rate				125	kHz
Multiplexer Settling Time			500		ns
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
SWITCH DRIVERS					
On-Resistance					
Y+, X+			5		Ω
Y–, X–			6		Ω
Drive Current[2]	Duration 100ms			50	mA
REFERENCE OUTPUT					
Internal Reference Voltage		2.45	2.50	2.55	V
Internal Reference Drift			15		ppm/°C
Quiescent Current			500		µA

ELECTRICAL CHARACTERISTICS (Cont.)

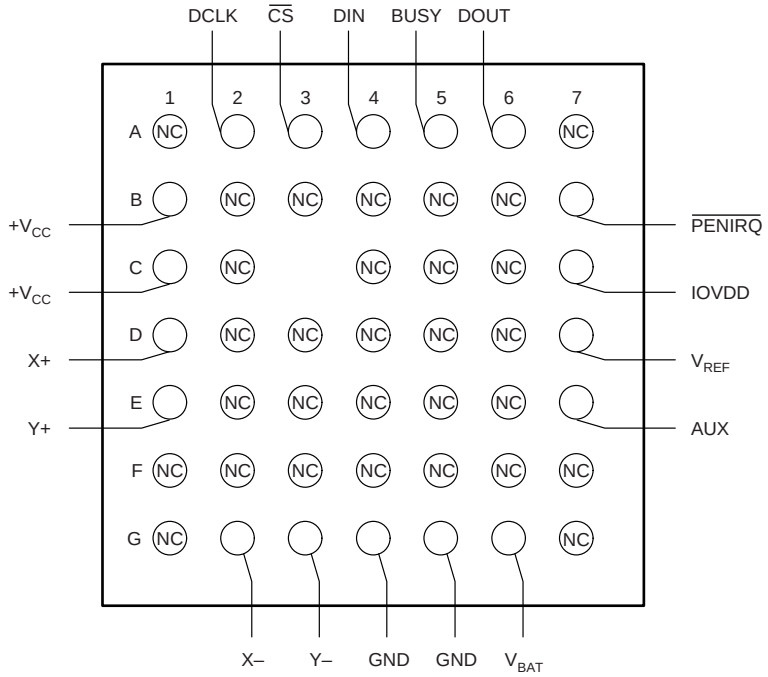
At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = 2.5V internal voltage, f_{SAMPLE} = 125kHz, f_{CLK} = 16 • f_{SAMPLE} = 2MHz, 12-bit mode, digital inputs = GND or IOVDD, and $+V_{CC}$ must be ≥ IOVDD, unless otherwise noted.

		TSC2046			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
REFERENCE INPUT					
Range		1.0		$+V_{CC}$	V
Input Impedance	SER/$\overline{DFR}$ = 0, PD1 = 0,		1		GΩ
	Internal Reference OFF				
	Internal Reference ON		250		Ω
BATTERY MONITOR					
Input Voltage Range		0.5		6.0	V
Input Impedance					
Sampling Battery			10		kΩ
Battery Monitor OFF			1		GΩ
Accuracy	V_{BAT} = 0.5V to 5.5V, External V_{REF} = 2.5V	–2		+2	%
	V_{BAT} = 0.5V to 5.5V, Internal Reference	–3		+3	%
TEMPERATURE MEASUREMENT					
Temperature Range		–40°C		+85	°C
Resolution	Differential Method(3)		1.6		°C
	TEMP0(4)		0.3		°C
Accuracy	Differential Method(3)		±2		°C
	TEMP0(4)		±3		°C
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
V_{IH}	| I_{IH} | ≤ +5µA	IOVDD • 0.7		IOVDD + 0.3	V
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		0.3 • IOVDD	V
V_{OH}	I_{OH} = –250µA	IOVDD • 0.8			V
V_{OL}	I_{OL} = 250µA			0.4	V
Data Format			Straight Binary		
POWER-SUPPLY REQUIREMENTS					
$+V_{CC}$(5)	Specified Performance	2.7		3.6	V
	Operating Range	2.2		5.25	V
IOVDD(6)		1.5		$+V_{CC}$	V
Quiescent Current(7)	Internal Reference OFF		280	650	µA
	Internal Reference ON		780		µA
	f_{SAMPLE} = 12.5kHz		220		µA
	Power-Down Mode with			3	µA
	$\overline{CS}$ = DCLK = DIN = IOVDD				
Power Dissipation	$+V_{CC}$ = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

NOTES: (1) LSB means Least Significant Bit. With V_{REF} = +2.5V, one LSB is 610µV. (2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation. (3) Difference between TEMP0 and TEMP1 measurement. No calibration necessary. (4) Temperature drift is –2.1mV/°C. (5) TSC2046 will operate down to 2.2V. (6) IOVDD must be ≤ $+V_{CC}$. (7) Combined supply current from $+V_{CC}$ and IOVDD. Typical values obtained from conversions on AUX input with PD0 = 0.

PIN CONFIGURATION

Top View **VFBGA**

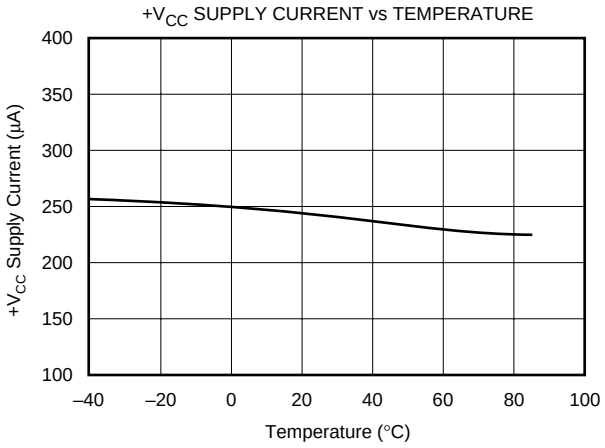


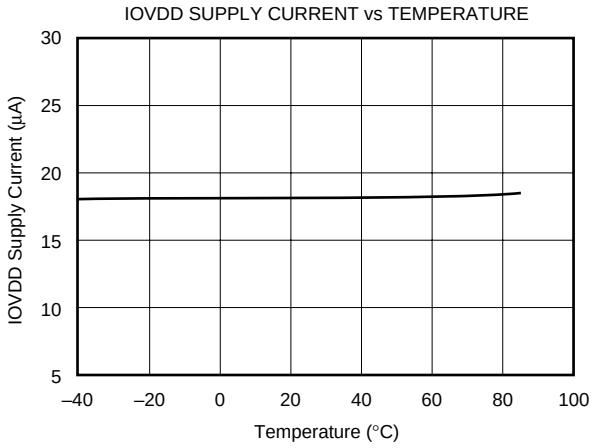
PIN DESCRIPTION

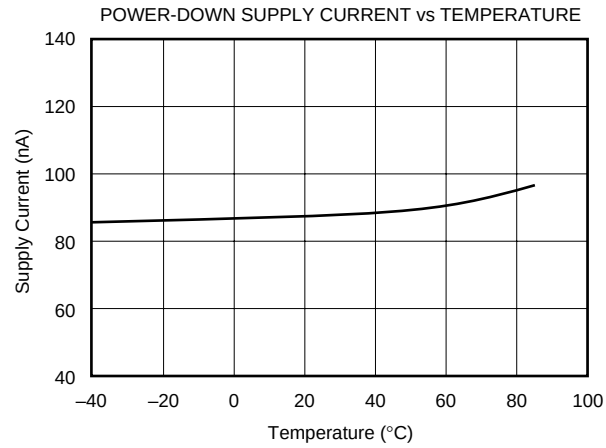
VFBGA PIN #	NAME	DESCRIPTION
B1 and C1	$+V_{CC}$	Power Supply
D1	X+	X+ Position Input
E1	Y+	Y+ Position Input
G2	X–	X– Position Input
G3	Y–	Y– Position Input
G4 and G5	GND	Ground
G6	V_{BAT}	Battery Monitor Input
E7	AUX	Auxiliary Input to ADC
D7	V_{REF}	Voltage Reference Input/Output
C7	IOVDD	Digital I/O Power Supply
B7	$\overline{\text{PENIRQ}}$	Pen Interrupt
A6	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{\text{CS}}$ is HIGH.
A5	BUSY	Busy Output. This output is high impedance when $\overline{\text{CS}}$ is HIGH.
A4	DIN	Serial Data Input. If $\overline{\text{CS}}$ is LOW, data is latched on rising edge of DCLK.
A3	$\overline{\text{CS}}$	Chip Select Input. Controls conversion timing and enables the serial input/output register. $\overline{\text{CS}}$ HIGH = power-down mode (ADC only).
A2	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

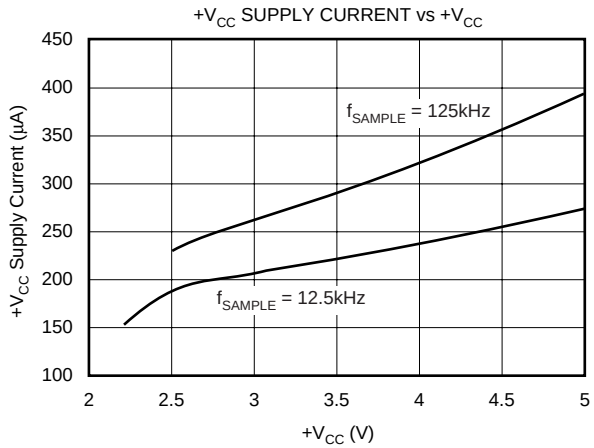
TYPICAL CHARACTERISTICS

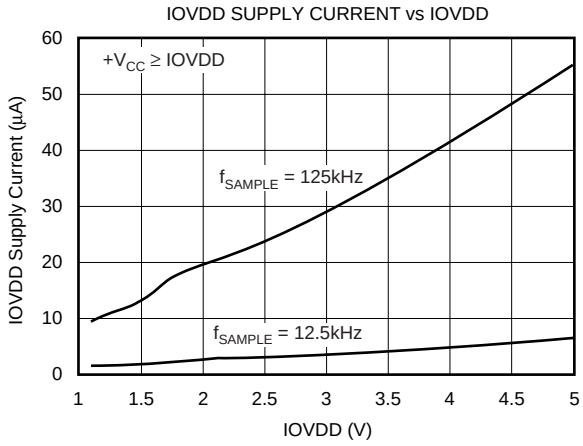
At T_A = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, V_{REF} = External +2.5V, 12-bit mode, PD0 = 0, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

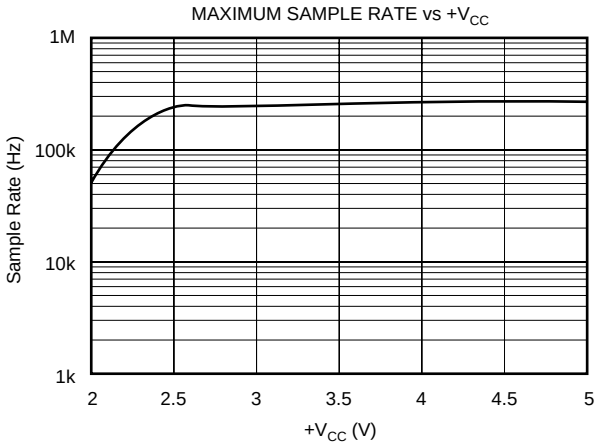








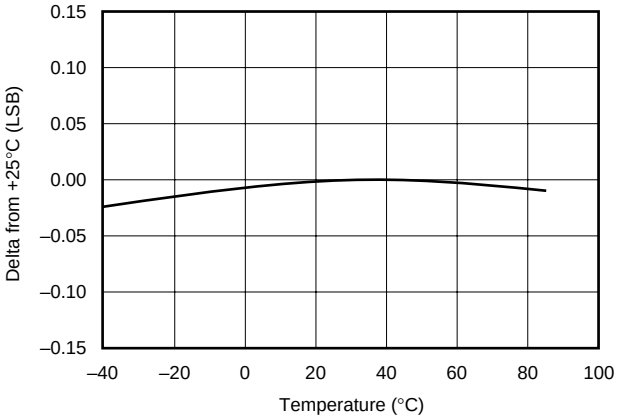




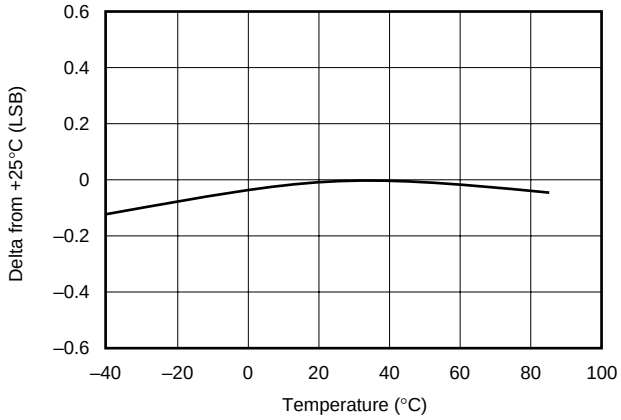
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, V_{REF} = External +2.5V, 12-bit mode, PD0 = 0, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

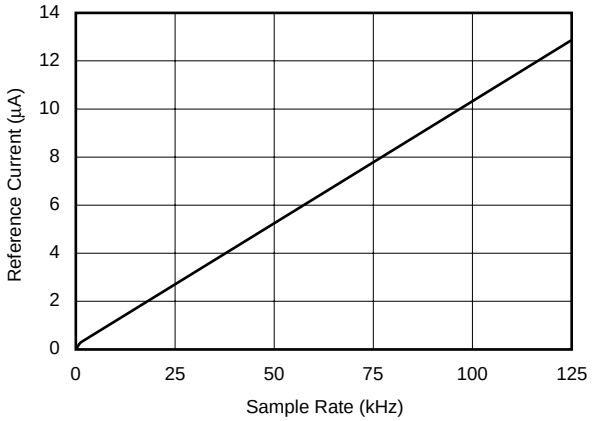
CHANGE IN GAIN vs TEMPERATURE



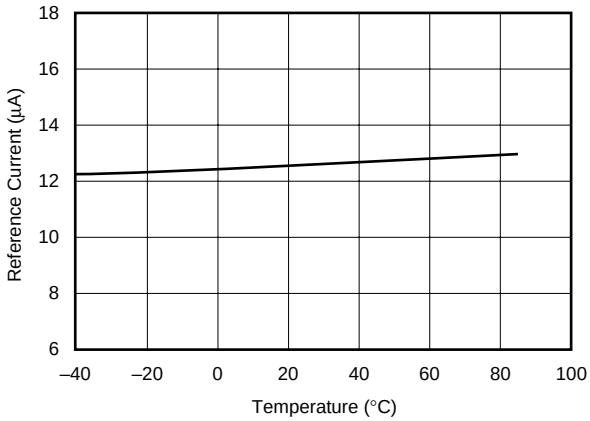
CHANGE IN OFFSET vs TEMPERATURE



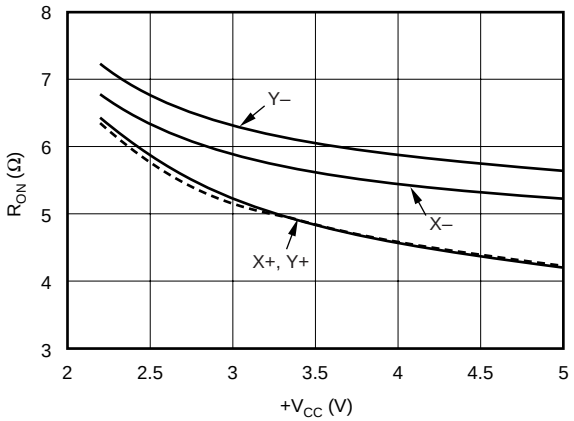
REFERENCE CURRENT vs SAMPLE RATE



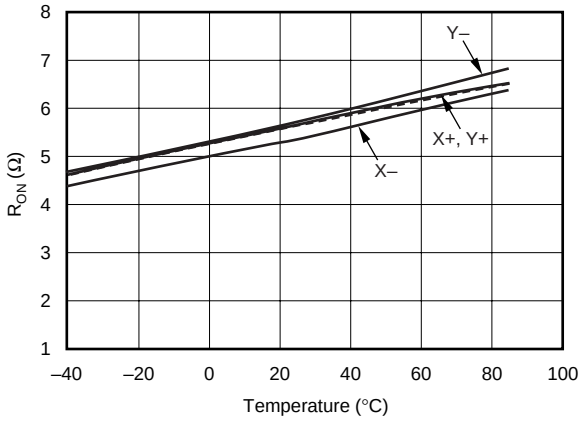
REFERENCE CURRENT vs TEMPERATURE



SWITCH ON-RESISTANCE vs $+V_{CC}$
($X+$, $Y+$: $+V_{CC}$ to Pin; $X–$, $Y–$: Pin to GND)



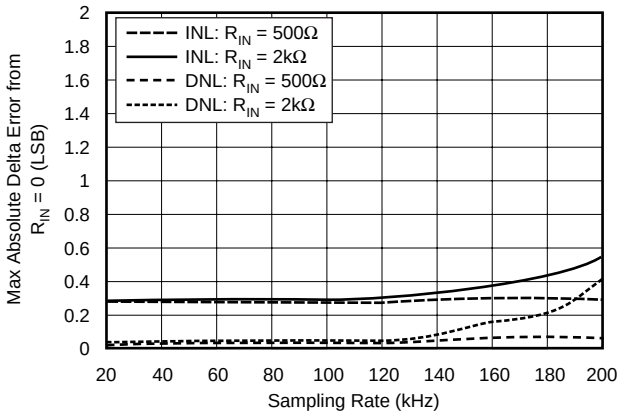
SWITCH ON-RESISTANCE vs TEMPERATURE
($X+$, $Y+$: $+V_{CC}$ to Pin; $X–$, $Y–$: Pin to GND)



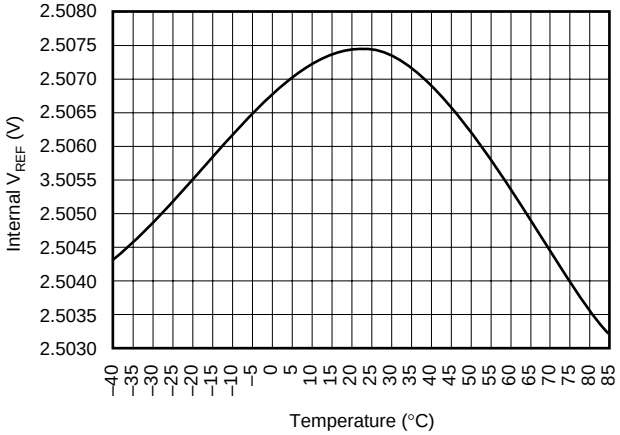
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, V_{REF} = External +2.5V, 12-bit mode, PD0 = 0, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

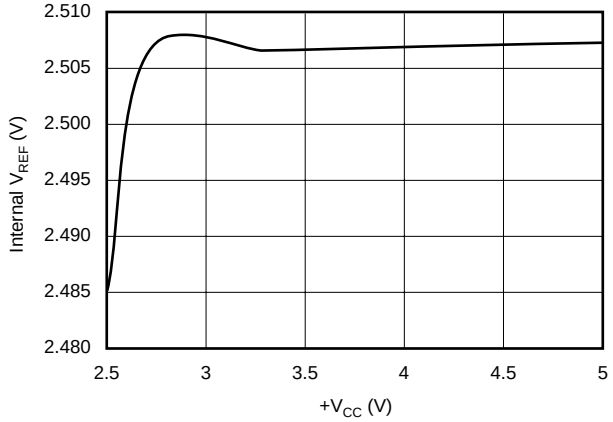
MAXIMUM SAMPLING RATE vs R_{IN}



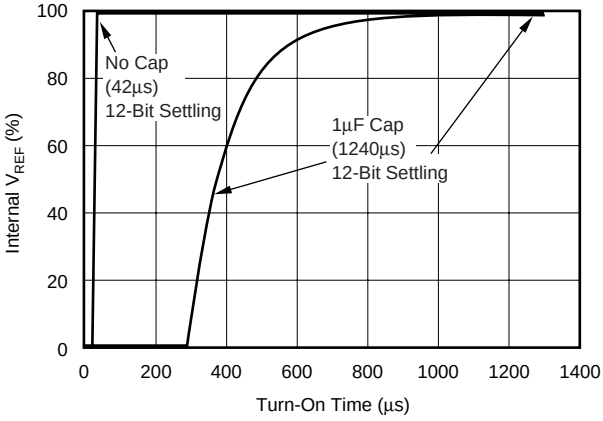
INTERNAL V_{REF} vs TEMPERATURE



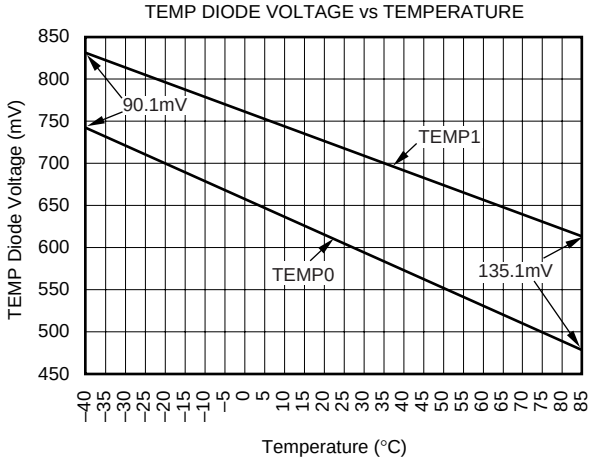
INTERNAL V_{REF} vs $+V_{CC}$



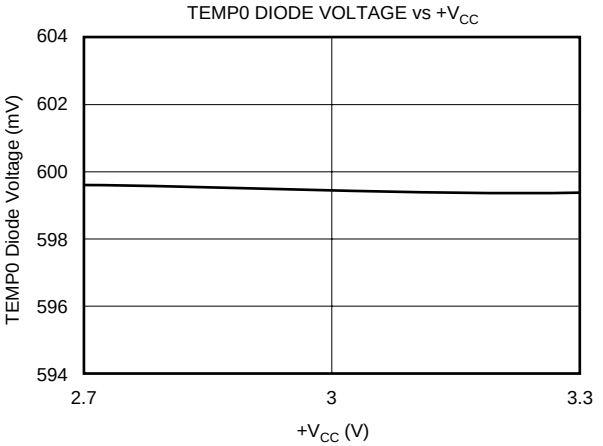
INTERNAL V_{REF} vs TURN-ON TIME



TEMP DIODE VOLTAGE vs TEMPERATURE

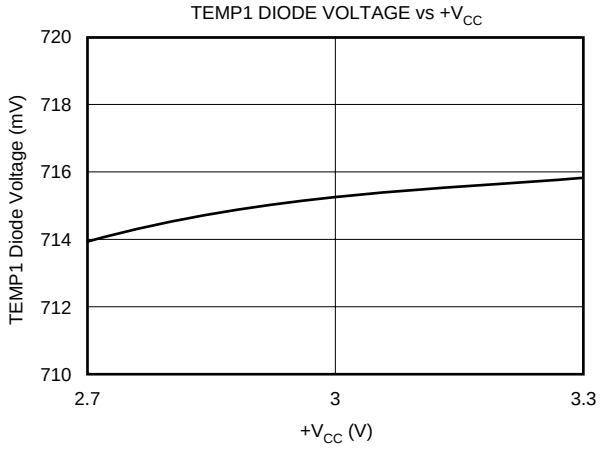


TEMP0 DIODE VOLTAGE vs $+V_{CC}$



TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, V_{REF} = External +2.5V, 12-bit mode, PD0 = 0, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.



THEORY OF OPERATION

The TSC2046 is a classic Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). The architecture is based on capacitive redistribution, which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µm CMOS process.

The basic operation of the TSC2046 is shown in Figure 1. The device features an internal 2.5V reference and uses an external clock. Operation is maintained from a single supply of 2.7V to 5.25V. The internal reference can be overdriven with an external, low-impedance source between 1V and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter.

The analog input (X-, Y-, and Z-Position coordinates, auxiliary input, battery voltage, and chip temperature) to the converter is provided via a multiplexer. A unique configuration of low on-resistance touch panel driver switches allows an unselected ADC input channel to provide power and its accompanying pin to provide ground for an external device, such as a touch screen. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the error from each touch panel driver switch's on-resistance (should this be a source of error for the particular measurement).

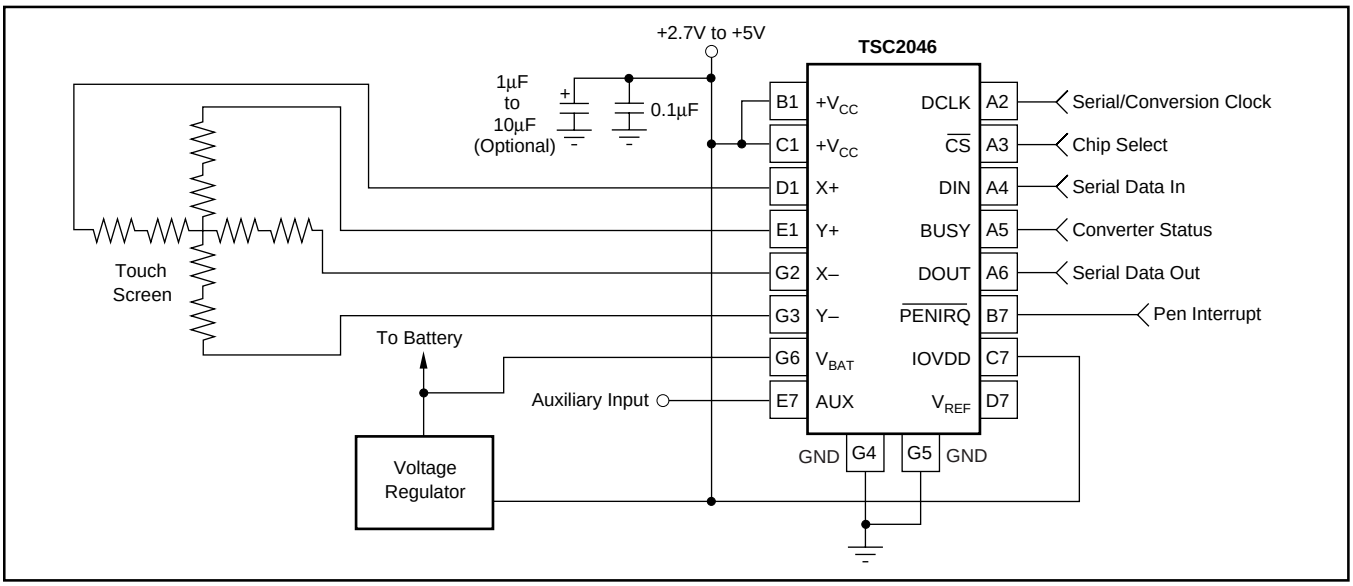


FIGURE 1. Basic Operation of the TSC2046.

ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the TSC2046, the differential input of the ADC, and the converter's differential reference. Table I and Table II show the relationship between the A2, A1, A0, and SER/$\overline{\text{DFR}}$ control bits and the configuration of the TSC2046. The control bits are provided serially via the DIN pin—see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (as shown in Figure 2) is captured on the internal capacitor array. The input current into the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

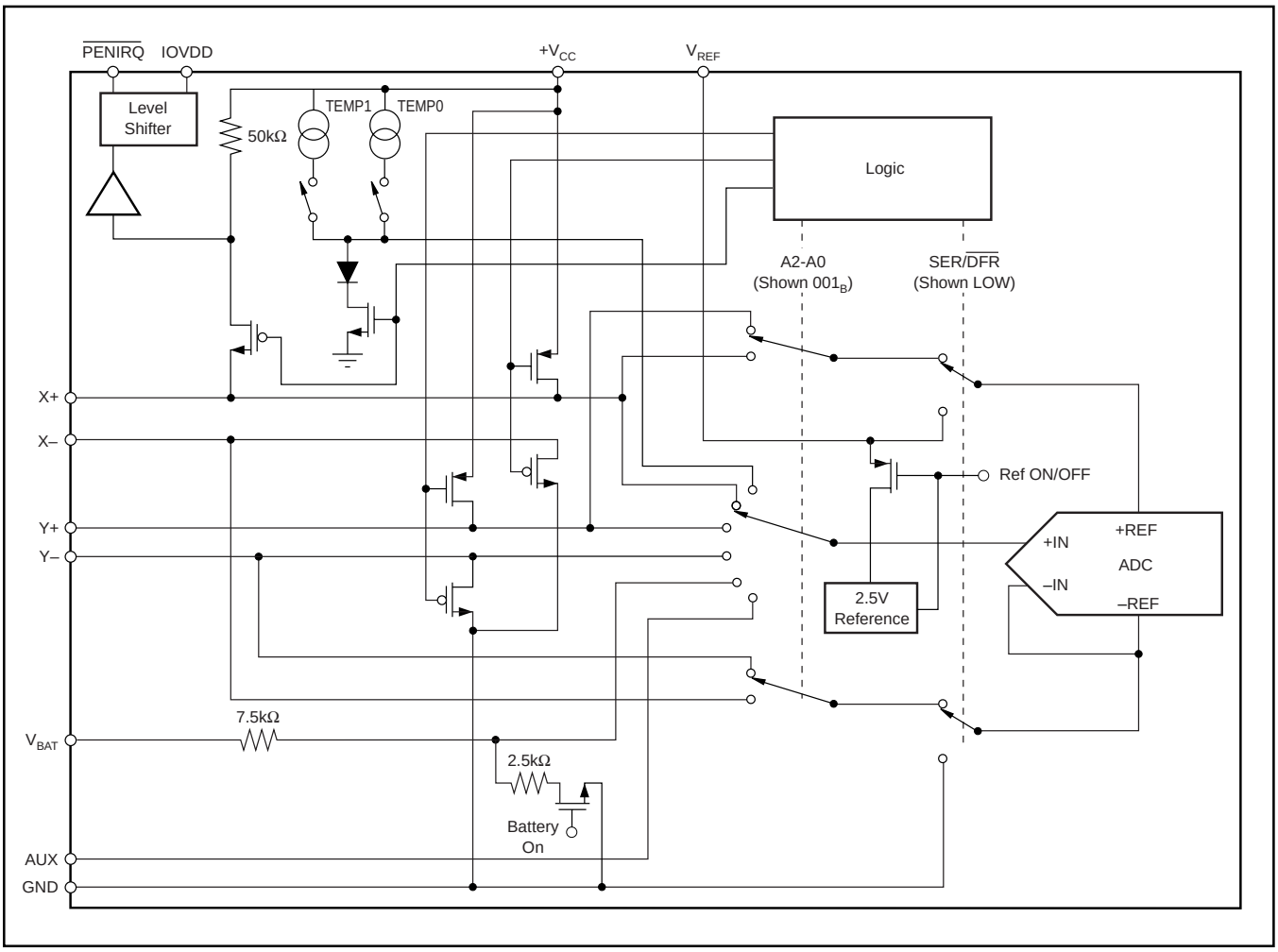


FIGURE 2. Simplified Diagram of Analog Input.

A2	A1	A0	V_{BAT}	AUX_{IN}	TEMP	Y–	X+	Y+	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	X-DRIVERS	Y-DRIVERS
0	0	0			+IN (TEMP0)								OFF	OFF
0	0	1					+IN		Measure				OFF	ON
0	1	0	+IN										OFF	OFF
0	1	1					+IN				Measure		X–, ON	Y+, ON
1	0	0				+IN						Measure	X–, ON	Y+, ON
1	0	1						+IN		Measure			ON	OFF
1	1	0		+IN									OFF	OFF
1	1	1			+IN (TEMP1)								OFF	OFF

TABLE I. Input Configuration (DIN), Single-Ended Reference Mode (SER/$\overline{\text{DFR}}$ HIGH).

A2	A1	A0	+REF	–REF	Y–	X+	Y+	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	DRIVERS ON
0	0	1	Y+	Y–		+IN		Measure				Y+, Y–
0	1	1	Y+	X–		+IN				Measure		Y+, X–
1	0	0	Y+	X–	+IN						Measure	Y+, X–
1	0	1	X+	X–			+IN		Measure			X+, X–

TABLE II. Input Configuration (DIN), Differential Reference Mode (SER/$\overline{\text{DFR}}$ LOW).

INTERNAL REFERENCE

The TSC2046 has an internal 2.5V voltage reference that can be turned ON or OFF with the control bit, PD1 (see Table V and Figure 3). Typically, the internal reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for utilizing the auxiliary input. Optimal touch screen performance is achieved when utilizing the differential mode. The internal reference voltage of the TSC2046 must be commanded to be OFF to maintain compatibility with the ADS7843. Therefore, after power-up, a write of PD1 = 0 is required to insure the reference is OFF. See the Typical Characteristics for power-up time of the reference from power-down.

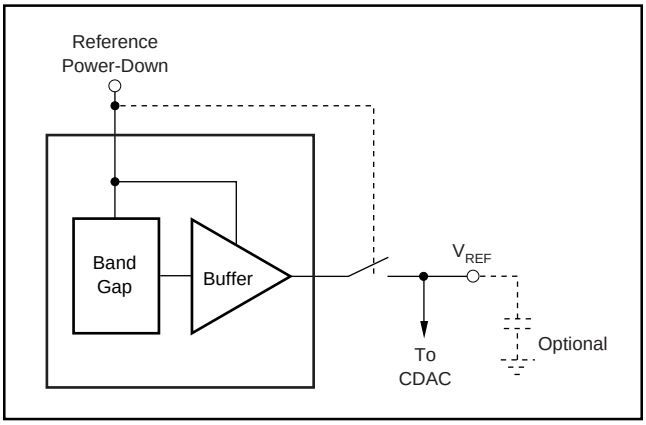


FIGURE 3. Simplified Diagram of the Internal Reference.

REFERENCE INPUT

The voltage difference between +REF and –REF (see Figure 2) sets the analog input range. The TSC2046 will operate with a reference in the range of 1V to $+V_{CC}$. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (Least Significant Bit) size and is equal to the reference voltage divided by 4096 in 12-bit mode. Any offset or gain error inherent in the ADC will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, it will typically be 5LSBs with a 1V reference. In each case, the actual offset of the device is the same: 1.22mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference (if an external reference is used), and a low-noise input signal.

The voltage into the V_{REF} input directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the TSC2046. Therefore, the input current is very low (typically < 13µA).

There is also a critical item regarding the reference when making measurements while the switch drivers are ON. For this discussion, it is useful to consider the basic operation of the TSC2046, as shown in Figure 1. This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y-Position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+ (Figure 4 shows a block diagram). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern). However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

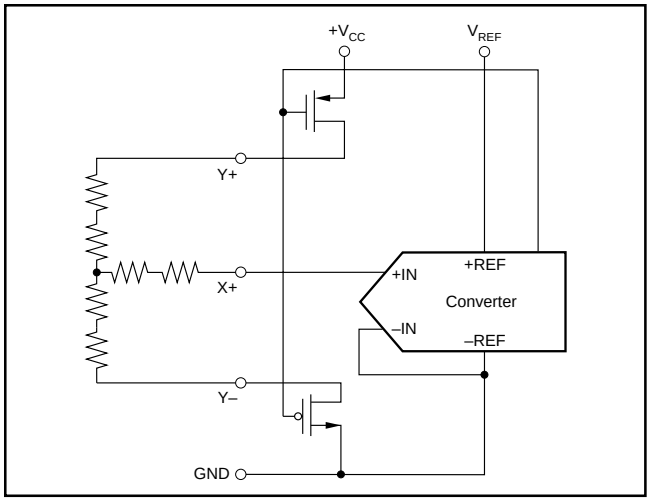


FIGURE 4. Simplified Diagram of Single-Ended Reference (SER/$\overline{\text{DFR}}$ HIGH, Y switches enabled, X+ is analog input).

This situation can be remedied as shown in Figure 5. By setting the SER/$\overline{\text{DFR}}$ bit LOW, the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This makes the analog-to-digital conversion ratiometric. The result of the conver-

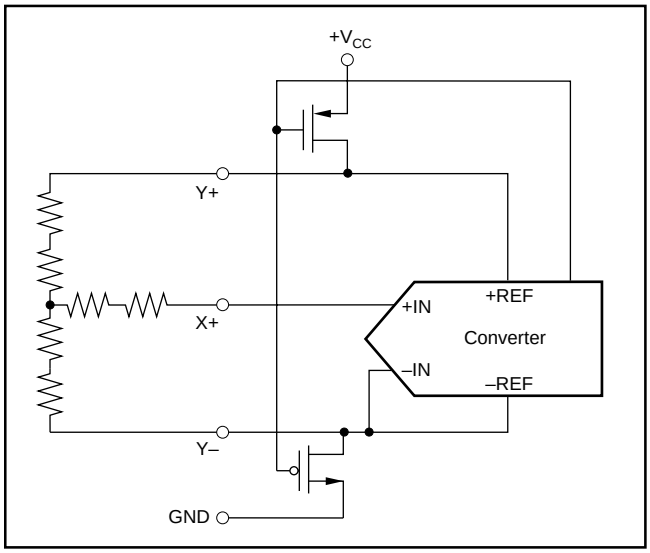


FIGURE 5. Simplified Diagram of Differential Reference (SER/$\overline{\text{DFR}}$ LOW, Y switches enabled, X+ is analog input).

sion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation (see the Power Dissipation section for more details).

As a final note about the differential reference mode, it must be used with $+V_{CC}$ as the source of the +REF voltage and cannot be used with V_{REF}. It is possible to use a high-precision reference on V_{REF} and single-ended reference mode for measurements which do not need to be ratiometric. In some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the TSC2046, but they might not be able to supply enough current for the external load (such as a resistive touch screen).

TOUCH SCREEN SETTLING

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (e.g., noise generated by the LCD panel or backlight circuitry). These capacitors will provide a low-pass filter to reduce the noise, but they will cause a settling time requirement when the panel is touched. The settling time will typically show up as a gain error. There are several methods for minimizing or eliminating this issue. The problem is the input and/or reference has not settled to its final steady-state value prior to the ADC sampling the input(s) and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle. Option 1 is to stop or slow down the TSC2046 DCLK for the required touch screen settling time. This will allow the input and reference to have stable values for the 'Acquire' period (3 clock cycles of the TSC2046; see Figure 9). This will work for both the single-ended and the differential modes. Option 2 is to operate the TSC2046 in the differential mode only for the touch screen measurements and command the TSC2046 to remain ON (touch screen drivers ON) and not go into power-down (PD0 = 1). Several conversions will be necessary depending on the settling time required and TSC2046 data rate. Once the required number of conversions have been made, the processor will command the TSC2046 to go into its power-down state on the last measurement. This process would be required for X-Position, Y-Position, and Z-Position measurements. Option 3 is to operate in the 15 Clock-per-Conversion mode, which overlaps the analog-to-digital conversions and maintains the touch screen drivers ON until it is commanded to stop by the processor (see Figure 13).

TEMPERATURE MEASUREMENT

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2046 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes. The TSC2046 offers two modes of operation. The first mode requires calibration at a known temperature, but it only requires a single reading to predict the ambient temperature. A diode is used (turned ON) during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the forward bias voltage by the ADC with an address of A2 = 0, A1 = 0, and A0 = 0 (see Table I and Figure 6 for details). This voltage is typically 600mV at +25°C with a 20μA current through the diode. The absolute value of this diode voltage can vary a few millivolts. However, the TC of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (in 12-bit mode).

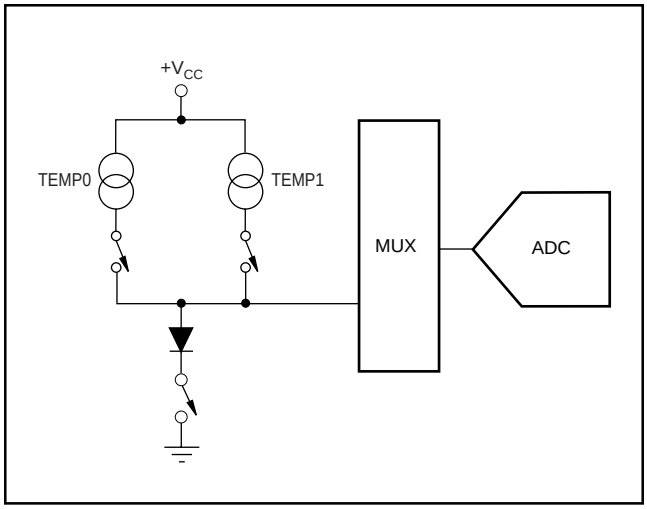


FIGURE 6. Functional Block Diagram of Temperature Measurement Mode.

The second mode does not require a test temperature calibration, but it uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2°C accuracy. This mode requires a second conversion with an address of A2 = 1, A1 = 1, and A0 = 1, with a 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current will be represented by kT/q • ln(N), where N is the current ratio = 91, k = Boltzmann's constant ($1.38054 \bullet 10^{-23}$ electron volts/degrees Kelvin), q = the electron charge ($1.602189 \bullet 10^{-19}$ C), and T = the temperature in degrees Kelvin. This method can provide improved absolute temperature measurement over the first mode at the cost of less resolution (1.6°C/LSB). The equation for solving for °K is:

$$°K = q \bullet \Delta V/(k \bullet \ln(N)) \quad (1)$$

where, $\Delta V = V(I_{91}) - V(I_1)$ (in mV)

$\therefore$ °K = 2.573 °K/mV • ΔV

°C = 2.573 • ΔV(mV) – 273°K

NOTE: The bias current for each diode temperature measurement is only ON for 3 clock cycles (during the acquisition mode) and, therefore, does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

BATTERY MEASUREMENT

An added feature of the TSC2046 is the ability to monitor the battery voltage on the other side of the voltage regulator (DC/DC converter), as shown in Figure 7. The battery voltage can vary from 0V to 6V, while maintaining the voltage to the TSC2046 at 2.7V, 3.3V, etc. The input voltage (V_{BAT}) is divided down by 4 so that a 5.5V battery voltage is represented as 1.375V to the ADC. This simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only ON during the sampling period when A2 = 0, A1 = 1, and A0 = 0. See Table I for the relationship between the control bits and configuration of the TSC2046.

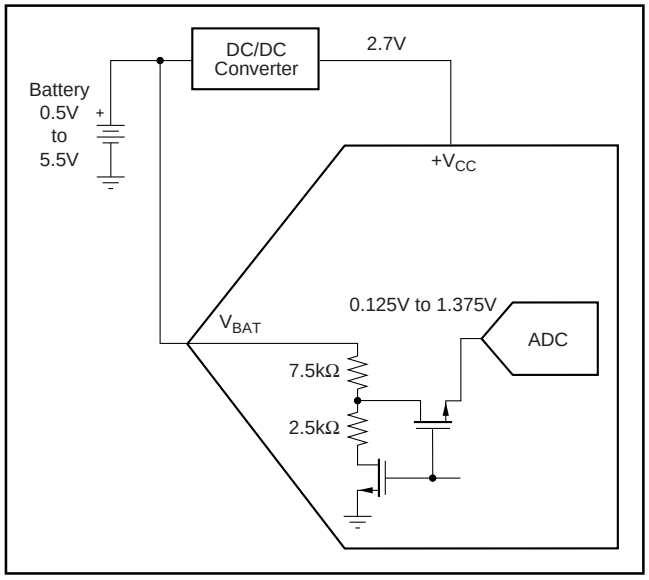


FIGURE 7. Battery Measurement Functional Block Diagram.

PRESSURE MEASUREMENT

Measuring touch pressure can also be done with the TSC2046. To determine pen or finger touch, the pressure of the "touch" needs to be determined. Generally, it is not necessary to have very high performance for this test, therefore, the 8-bit resolution mode is recommended (however, calculations will be shown here using the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2046 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross panel measurements (Z_1 and Z_2) of the touch screen, as shown in Figure 8. Using Equation 2 will calculate the touch resistance:

$$R_{TOUCH} = R_{X-plate} \bullet \frac{X-Position}{4096}\left(\frac{Z_2}{Z_1}-1\right) \qquad (2)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Using Equation 3 will also calculate the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \bullet X-Position}{4096}\left(\frac{4096}{Z_1}-1\right) - R_{Y-plate}\left(1-\frac{Y-Position}{4096}\right) \qquad (3)$$

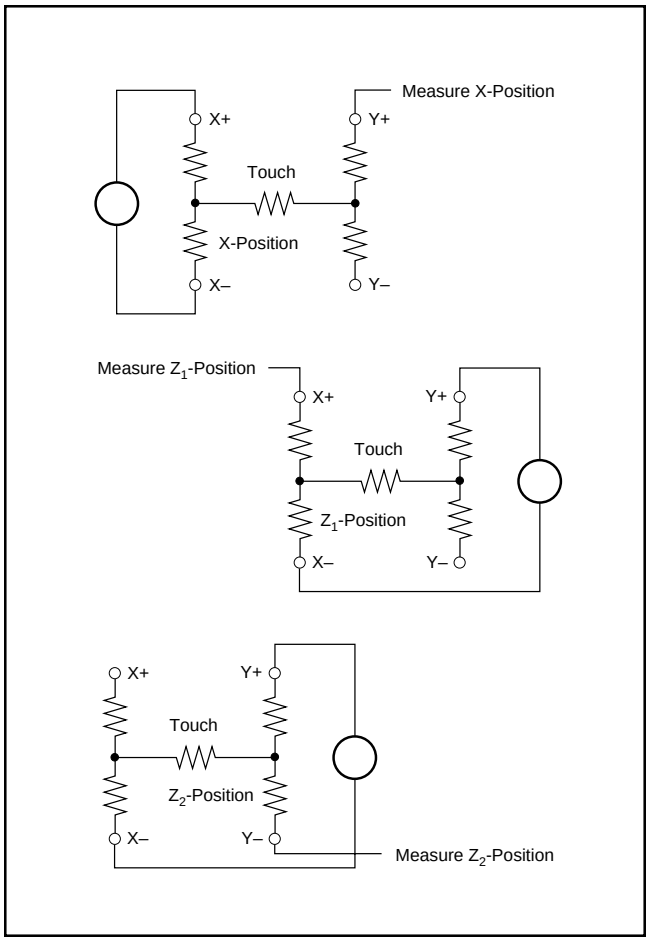


FIGURE 8. Pressure Measurement Block Diagrams.

DIGITAL INTERFACE

See Figure 9 for the typical operation of the TSC2046's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter, such as SPI, SSI, or Microwire™ synchronous serial interface, consists of eight clock cycles. One complete conversion can be accomplished with three serial communications for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the touch panel drivers are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the touch panel drivers may turn OFF (in single-ended mode). The next 12 clock cycles accomplish the actual analog-to-digital conversion. If the conversion is ratiometric ($SER/\overline{DFR}$ = 0), the drivers are on during the conversion. A 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

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Control Byte

The control byte (on DIN), as shown in Table III, provides the start conversion, addressing, ADC resolution, configuration, and power-down of the TSC2046. Figure 9 and Tables III and IV give detailed information regarding the order and description of these control bits within the control byte.

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode (see Figure 13).
6-4	A2-A0	Channel Select bits. Along with the SER/$\overline{\text{DFR}}$ bit, these bits control the setting of the multiplexer input, touch driver switches, and reference inputs (see Tables I and II).
3	MODE	12-Bit/8-Bit Conversion Select bit. This bit controls the number of bits for the next conversion: 12-bits (LOW) or 8-bits (HIGH).
2	SER/$\overline{\text{DFR}}$	Single-Ended/Differential Reference Select bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, touch driver switches, and reference inputs (see Tables I and II).
1-0	PD1-PD0	Power-Down Mode Select bits. Refer to Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

Initiate START—The first bit, the “S” bit, must always be HIGH and initiates the start of the control byte. The TSC2046 will ignore inputs on the DIN pin until the start bit is detected.

Addressing—The next three bits (A2, A1, and A0) select the active input channel(s) of the input multiplexer (see Tables I, II, and Figure 2), touch screen drivers, and the reference inputs.

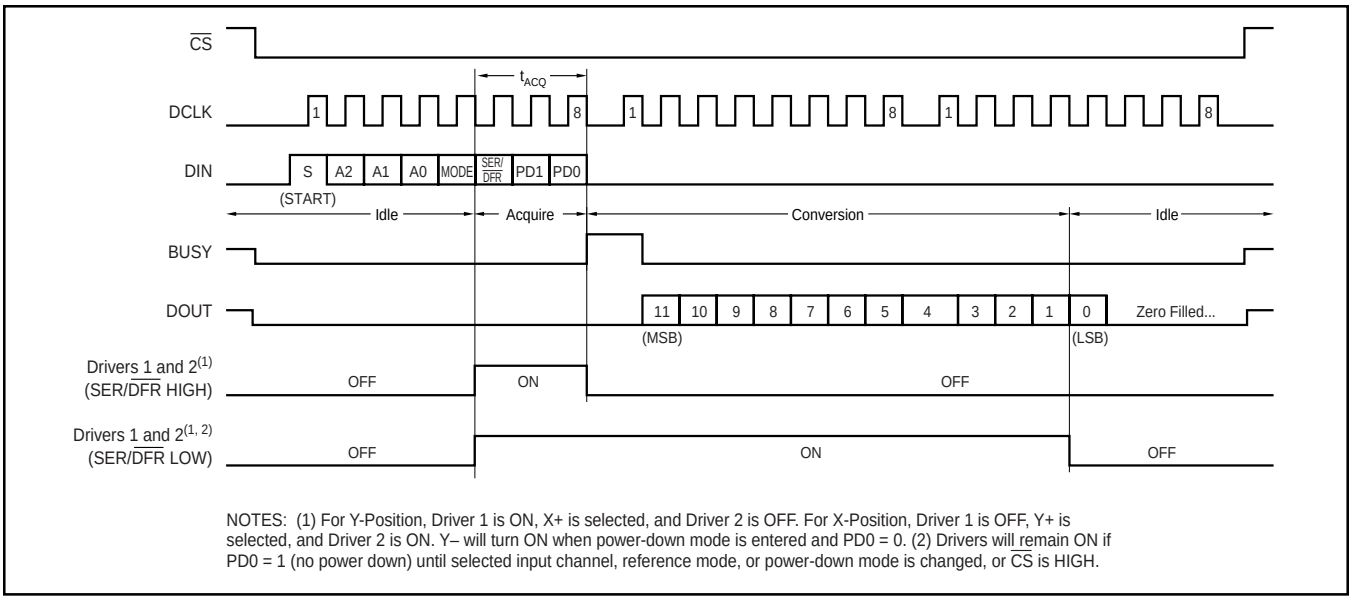
MODE—The mode bit sets the resolution of the ADC. With this bit LOW, the next conversion will be 12 bits of resolution. With this bit HIGH, the next conversion will be 8 bits of resolution.

SER/$\overline{\text{DFR}}$—The SER/$\overline{\text{DFR}}$ bit controls the reference mode, either single-ended (HIGH) or differential (LOW). The differential mode is also referred to as the ratiometric conversion mode. The differential mode is preferred for X-Position, Y-Position, and Pressure-Touch measurements for optimum performance. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a reference voltage is not needed as the reference voltage to the ADC is the voltage across the touch screen. In the single-ended mode, the converter’s reference voltage is always the difference between the V_{REF} and GND pins. See Tables I and II, and Figures 2 through 5 for further information.

If X-Position, Y-Position, and Pressure-Touch are measured in the single-ended mode, an external reference voltage is needed. The TSC2046 should also be powered from the external reference. Caution should be observed when utilizing the single-ended mode such that the input voltage to the ADC does not exceed the internal reference voltage, especially if the supply voltage is greater than 2.7V.

NOTE: The differential mode can only be used for X-Position, Y-Position, and Pressure-Touch measurements. All other measurements require the single-ended mode.

PD0 and PD1—Table V describes the power-down and the internal reference voltage configurations. The internal reference voltage can be turned ON or OFF independently of the ADC. This can allow extra time for the internal reference voltage to settle to its final value prior to making a conversion. Make sure to also allow this extra wake-up time if the internal reference was powered down. The ADC requires no wake-up time and can be instantaneously used. Also note that the



NOTES: (1) For Y-Position, Driver 1 is ON, X+ is selected, and Driver 2 is OFF. For X-Position, Driver 1 is OFF, Y+ is selected, and Driver 2 is ON. Y– will turn ON when power-down mode is entered and PD0 = 0. (2) Drivers will remain ON if PD0 = 1 (no power down) until selected input channel, reference mode, or power-down mode is changed, or $\overline{\text{CS}}$ is HIGH.

FIGURE 9. Conversion Timing, 24 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-Down Between Conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid. The Y– switch is ON while in power-down.
0	1	Disabled	Reference is OFF and ADC is ON.
1	0	Enabled	Reference is ON and ADC is OFF.
1	1	Disabled	Device is always powered. Reference is ON and ADC is ON.

TABLE V. Power-Down and Internal Reference Selection.

status of the internal reference power-down is latched into the part (internally) with BUSY going HIGH. In order to turn the reference OFF, an additional write to the TSC2046 is required after the channel has been converted.

$\overline{\text{PENIRQ}}$ OUTPUT

The pen-interrupt output function is shown in Figure 10. While in power-down mode with PD0 = 0, the Y– driver is ON and connects the Y-plane of the touch screen to GND. The $\overline{\text{PENIRQ}}$ output is connected to the X+ input through two transmission gates. When the screen is touched, the X+ input is pulled to ground through the touch screen. The $\overline{\text{PENIRQ}}$ output goes LOW due to the current path through the touch screen to ground, which initiates an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input will be disconnected from the $\overline{\text{PENIRQ}}$ internal pull-up resistor. This is done to eliminate any leakage current from the internal pull-up resistor through the touch screen, thus causing no errors.

Furthermore, the $\overline{\text{PENIRQ}}$ output will be disabled and LOW during the measurement cycle for X-, Y-, and Z-Position. The $\overline{\text{PENIRQ}}$ output will be disabled and HIGH during the measurement cycle for battery monitor, auxiliary input, and chip temperature. If the last control byte written to the TSC2046 contains PD0 = 1, the pen-interrupt output function will be disabled and will not be able to detect when the screen is touched. In order to re-enable the pen-interrupt output function

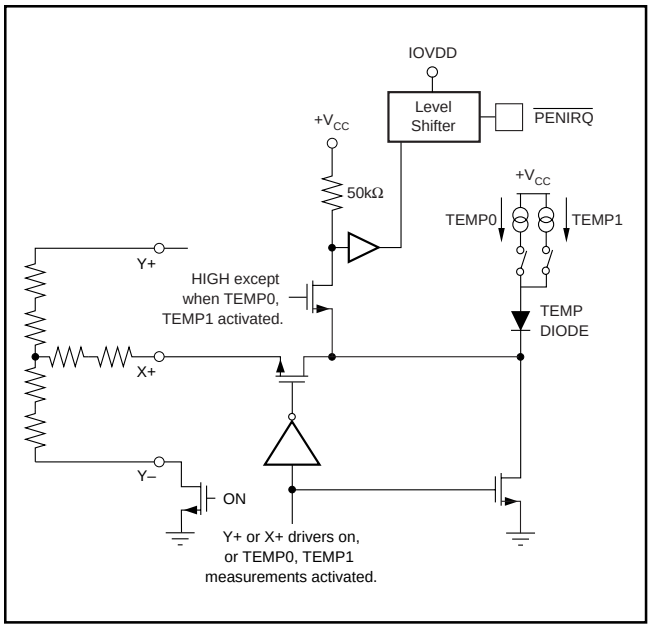


FIGURE 10. $\overline{\text{PENIRQ}}$ Functional Block Diagram.

under these circumstances, a control byte needs to be written to the TSC2046 with PD0 = 0. If the last control byte written to the TSC2046 contains PD0 = 0, the pen-interrupt output function will be enabled at the end of the conversion. The end of the conversion occurs on the falling edge of DCLK after bit 1 of the converted data has been clocked out of the TSC2046.

It is recommended that the processor mask the interrupt $\overline{\text{PENIRQ}}$ is associated with whenever the processor sends a control byte to the TSC2046. This will prevent false triggering of interrupts when the $\overline{\text{PENIRQ}}$ output is disabled in the cases discussed in this section.

16 Clocks per Conversion

The control bits for conversion 'n + 1' can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 11. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer from the processor to the converter. This is possible, provided that each conversion completes

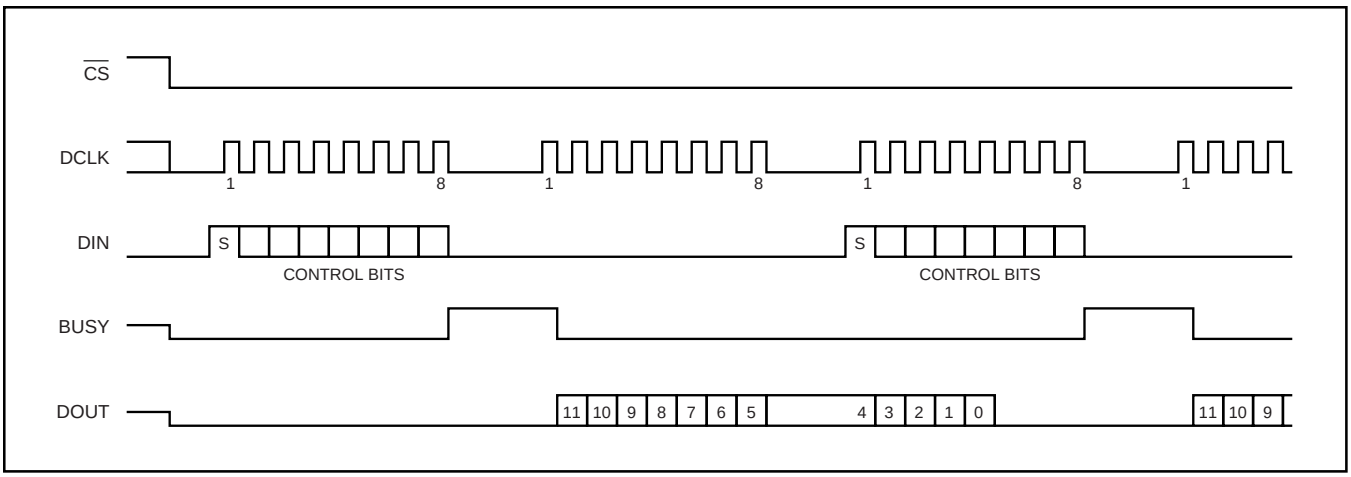


FIGURE 11. Conversion Timing, 16 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the TSC2046 is fully powered while other serial communications are taking place during a conversion.

Digital Timing

Figures 9 and 12 and Table VI provide detailed timing for the digital interface of the TSC2046.

15 Clocks per Conversion

Figure 13 provides the fastest way to clock the TSC2046. This method will not work with the serial interface of most microcontrollers and digital signal processors, as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated Circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

SYMBOL	DESCRIPTION	$+V_{CC} \geq 2.7V$, $+V_{CC} \geq IOVDD \geq 1.5V$, $C_{LOAD} = 50pF$			UNITS
		MIN	TYP	MAX	
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	50			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	10			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising/Falling			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications, T_A = –40°C to +85°C.

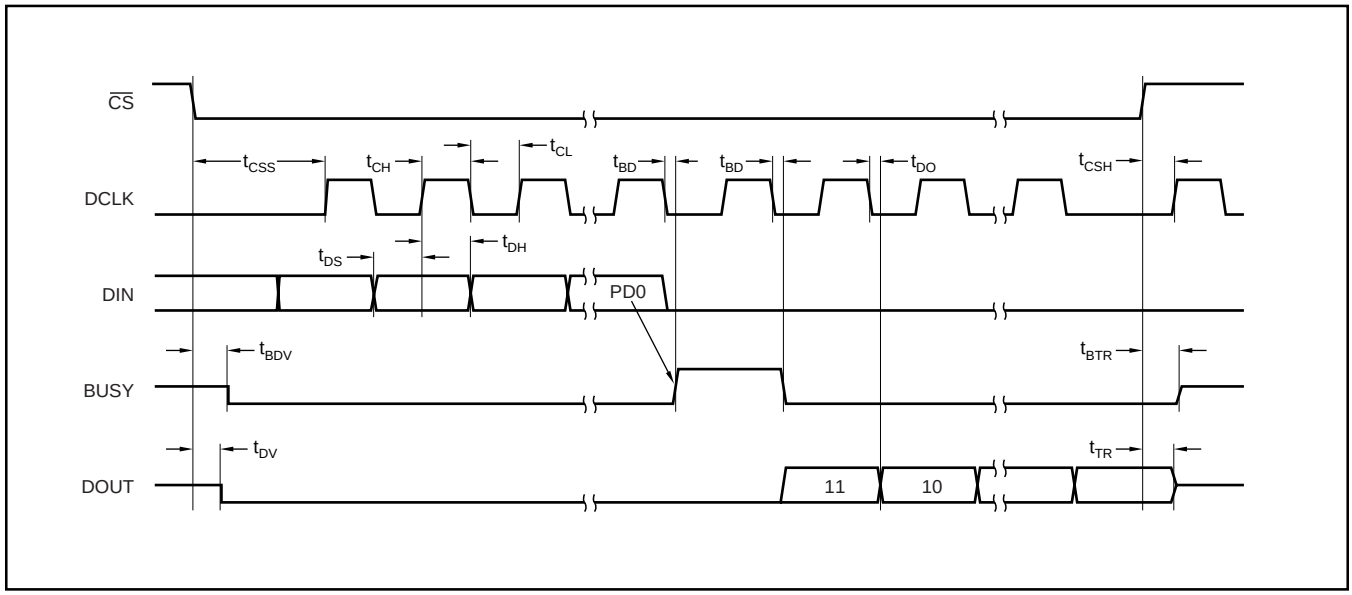


FIGURE 12. Detailed Timing Diagram.

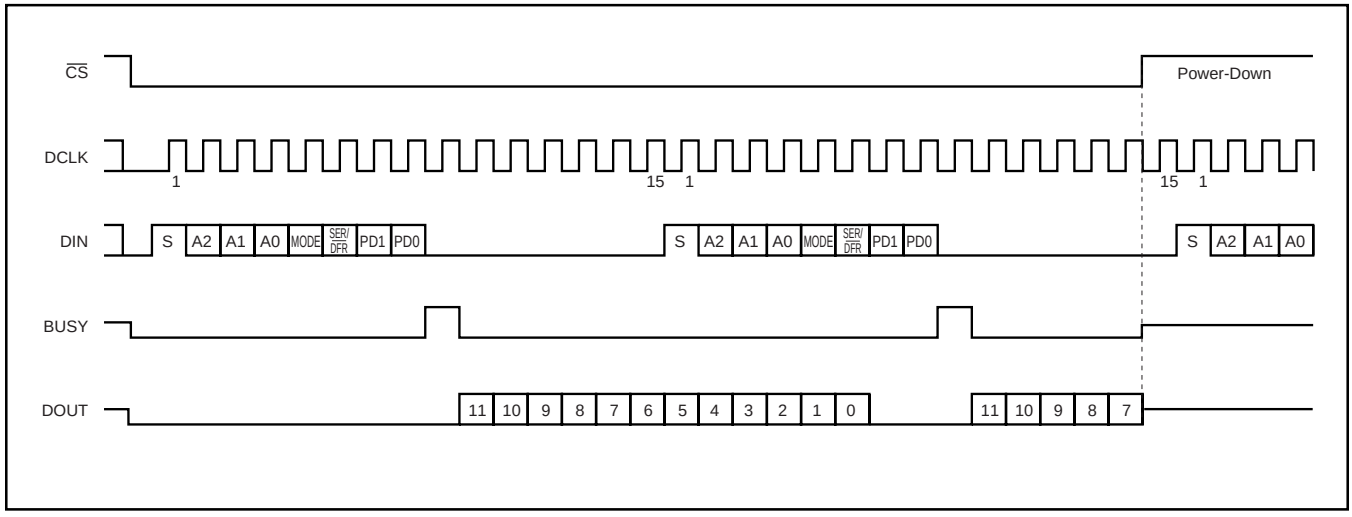
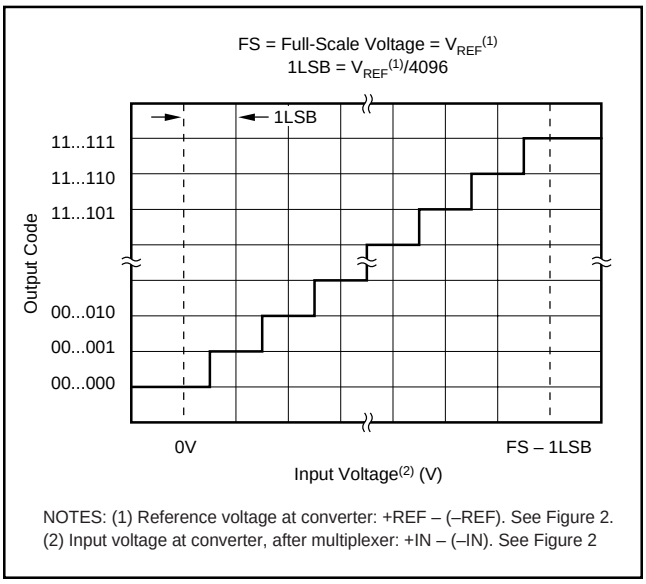


FIGURE 13. Maximum Conversion Rate, 15 Clocks per Conversion.

Data Format

The TSC2046 output data is in Straight Binary format, as shown in Figure 14. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTES: (1) Reference voltage at converter: +REF – (–REF). See Figure 2.
(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 2

FIGURE 14. Ideal Input Voltages and Output Codes.

8-Bit Conversion

The TSC2046 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the TSC2046 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

POWER DISSIPATION

There are two major power modes for the TSC2046: full-power (PD0 = 1) and auto power-down (PD0 = 0). When operating at full speed and 16 clocks-per-conversion (see Figure 11), the TSC2046 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are simply done less often, the difference between the two modes is dramatic.

Figure 15 shows the difference between reducing the DCLK frequency (“scaling” DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

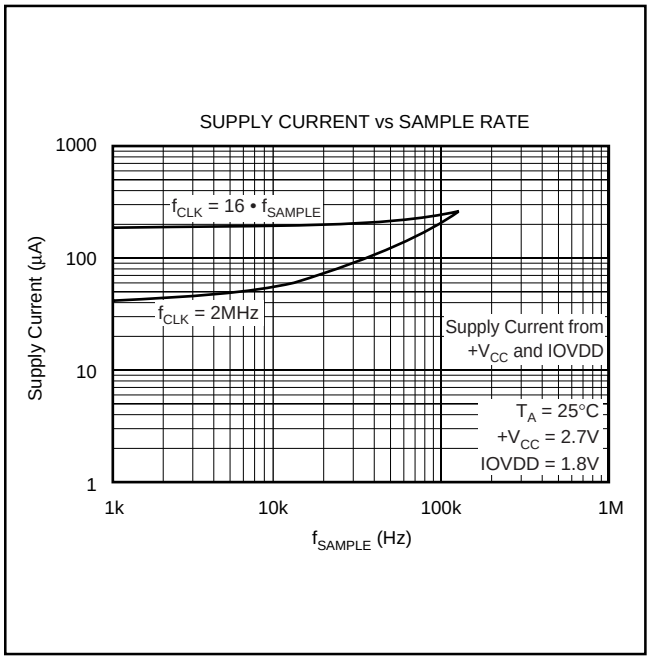


FIGURE 15. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Maintaining DCLK at the Maximum Possible Frequency.

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the touch panel drivers are ON only when the analog input voltage is being acquired (see Figure 9 and Table I). The external device (e.g., a resistive touch screen), therefore, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 9). If the conversion rate is high, this could substantially increase power dissipation.

$\overline{CS}$ will also put the TSC2046 into power-down mode. When $\overline{CS}$ goes HIGH, the TSC2046 immediately goes into power-down mode and does not complete the current conversion. The internal reference, however, does not turn OFF with $\overline{CS}$ going HIGH. To turn the reference OFF, an additional write is required before $\overline{CS}$ goes HIGH (PD1 = 0).

When the TSC2046 first powers up, the device will draw about 20µA of current until a control byte is written to it with PD0 = 0 to put it into power-down mode. This can be avoided if the TSC2046 is powered up with $\overline{CS}$ = 0 and DCLK = IOVDD.

LAYOUT

The following layout suggestions should provide the most optimum performance from the TSC2046. Many portable applications, however, have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly “clean” power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter’s power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2046 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an ‘n-bit’ SAR converter, there are n ‘windows’ in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the TSC2046 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{CC}$ or IOVDD and the power supplies is high. Low-leakage capacitors should be used to minimize power dissipation through the bypass capacitors when the TSC2046 is in power-down mode.

A bypass capacitor is generally not needed on the V_{REF} pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

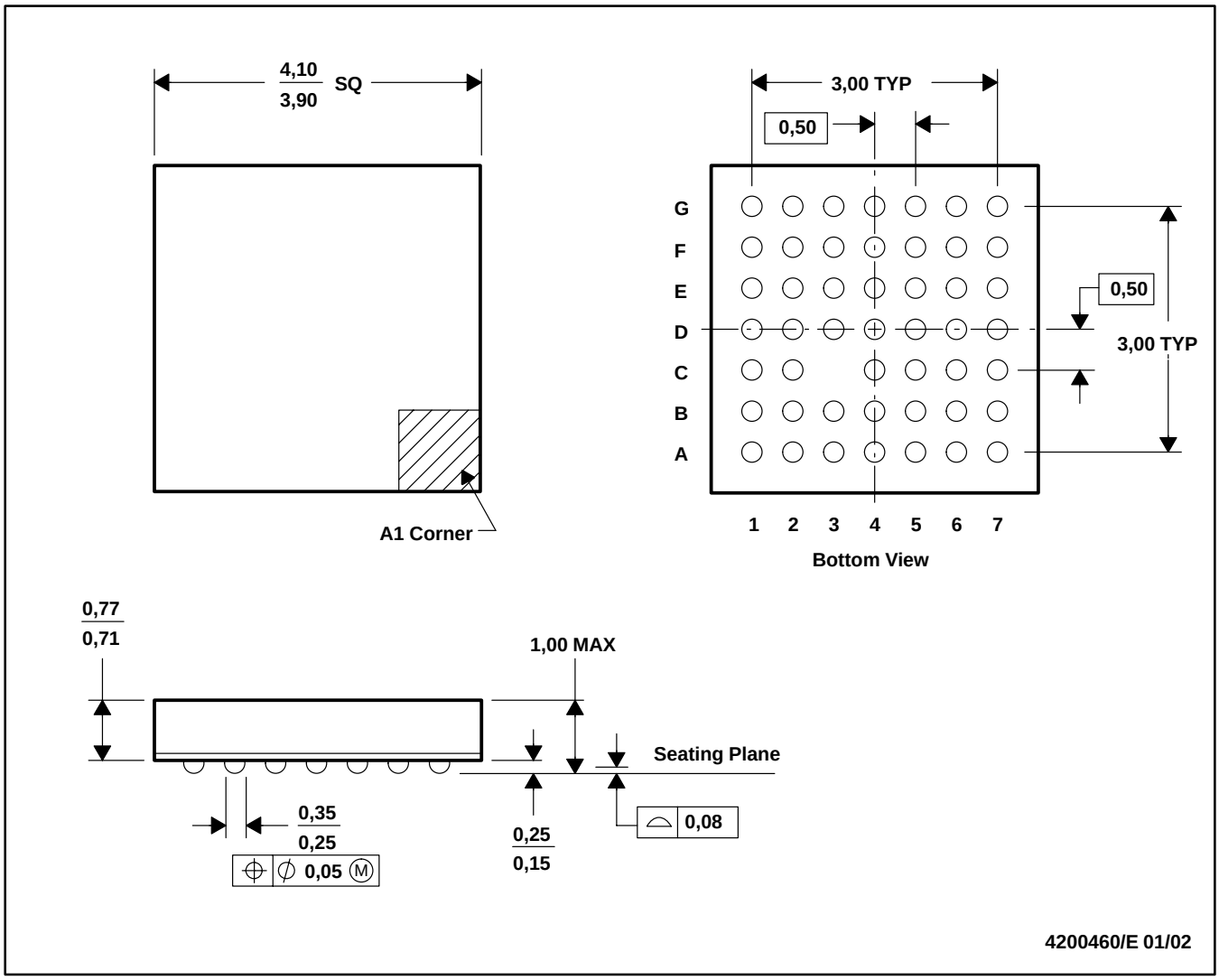
The TSC2046 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery-connection point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections will be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause “flickering” of the converted data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This will couple the majority of noise to ground. Additionally, filtering capacitors from Y+, Y–, X+, and X– pins to ground can also help. Caution should be observed under these circumstances for settling time of the touch screen, especially operating in the single-ended mode and at high data rates.

GQC (S-PBGA-N48) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior ™ BGA configuration
D. Falls within JEDEC MO-225

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